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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/678,609	Applicant(s) HONDA, HIROKAZU	
	Examiner David E Graybill	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Applicant's election without traverse of group I, claims 1-59 in Paper No. 4 is acknowledged.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 37, 38-42 and 44-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 37, there is insufficient literal antecedent basis for the limitation, "said supporting layer."

In claims 38 and 45, the limitation, "wherein said at least semiconductor chip is bonded via bumps to said second surface of said interconnection board," appears to be incompatible with the claims 18 and 43 limitation, "at least a semiconductor chip mounted on said first surface of said interconnection board."

In claims 44 and 49, there is insufficient literal antecedent basis for the limitation, "said buffer layer."

Claims 37, 44 and 49 have not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the

proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. See also MPEP 2173.06.

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being

examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 5-10 and 12-17 are rejected under 35 U.S.C. 102(a) as being anticipated by Tsukamoto (5841194).

At column 4, line 59 to column 6, line 61; and column 7, line 10 to column 8, line 54, Tsukamoto teaches the following:

1. A semiconductor device comprising an interconnection board 108; and

a high rigidity plate 106 securely fixed to said interconnection board, said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent.

2. The semiconductor device as in 1, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

3. The semiconductor device as in 1, wherein said high rigidity plate is made of a metal.

5. The semiconductor device as in 1, wherein said high rigidity plate is made of a ceramic.

6. The semiconductor device as in 1, wherein a base material of said interconnection board is an organic insulative material.

7. The semiconductor device as in 6, wherein said organic material is a polymer resin material.

8. A semiconductor device comprising an interconnection board having first and second surfaces; at least a semiconductor chip 201 mounted on said first surface of said interconnection board; and a high rigidity plate securely fixed to said second surface of said interconnection board, said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent.

9. The semiconductor device as in 8, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

10. The semiconductor device as in 8, wherein said high rigidity plate is made of a metal.

12. The semiconductor device as in 8, wherein said high rigidity plate is made of a ceramic.

13. The semiconductor device as in 8, wherein a base material of said interconnection board is an organic material.

14. The semiconductor device as in 13, wherein said organic material is a polymer resin material.

15. The semiconductor device as in 8, wherein said at least semiconductor chip is bonded via bumps 204 to said second surface of said interconnection board.

16. The semiconductor device as in 15, wherein further comprising a sealing resin material 205 provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

17. The semiconductor device as in 16, further comprising at least a heat spreader 601 provided on said at least semiconductor chip.

Claims 1, 4, 8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Farquhar (6329713).

At column 3, line 64 to column 4, line 1; and column 4, lines 36-67, Farquhar teaches the following:

1. A semiconductor device comprising an interconnection board 1; and

a high rigidity plate 8 securely fixed to said interconnection board, said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent.

4. The semiconductor device as in 1, wherein said high rigidity plate is made of an alloy ["Invar"].

8. A semiconductor device comprising an interconnection board having first and second surfaces; at least a semiconductor chip 3 mounted on said first surface of said interconnection board; and a high rigidity plate securely fixed to said second surface

of said interconnection board, said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent.

11. The semiconductor device as in 8, wherein said high rigidity plate is made of an alloy.

Claims 18-36, 38-43, 45-48, and 50-59 are rejected under 35 U.S.C. 102(b) as being anticipated by Allen (4705205).

At column 1, line 10 to column 2, line 20; column 2, lines 46 to column 2, line 68; column 3, lines 42-49; column 4, lines 1-21; column 8, lines 32-40; column 8, lines 62-68; column 12, line 22 to column 13, line 46; column 13, line 66 to column 14, line 38; column 15, lines 8-45; column 16, lines 27-39; column 16, line 52 to column 17, line 18; column 18, lines 15-20; column 18, line 66 to column 19, line 16; column 20, lines 37-58; and column 21, lines 12-28, Allen teaches the following:

18. A semiconductor device comprising an interconnection board 32 having first and second surfaces; at least a semiconductor chip mounted on said interconnection board; and
a buffer layer 20 having a first surface in contact with said second surface of said interconnection board and also said buffer layer having a second surface on which at least an external electrode 28 is provided, and said buffer layer having at least an electrical contact 28 between said interconnection

board and said at least external electrode, and said buffer layer being capable of absorbing and/or relaxing a stress applied to said at least external electrode to make said interconnection board free from application of said stress.

20. The semiconductor device as in 18, wherein said at least external electrode comprises plural external electrodes.

22. The semiconductor device as in 18, wherein said external electrode comprises a pin electrode.

23. The semiconductor device as in 18, wherein said external electrode comprises a coil-spring electrode 62.

24. The semiconductor device as in 18, wherein said external electrode comprises a generally column shaped electrode.

25. The semiconductor device as in 24, wherein said generally column shaped electrode comprises a straight column shaped electrode which is uniform in horizontal cross sectional area from a bottom to a top thereof.

26. The semiconductor device as in 24, wherein said generally column shaped electrode comprises a center-pinched column shaped electrode which decreases in horizontal cross sectional area toward an intermediate level thereof.

27. The semiconductor device as in 18, wherein said buffer layer comprises

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad 10 of said interconnection board and a second end directly fixed said external electrode.

28. The semiconductor device as in 27, wherein said plural generally column shaped electrically conductive layers are made of a metal.

29. The semiconductor device as in 18, wherein said buffer layer comprises plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode; and an stress absorption layer 22 filling gaps between said plural generally column shaped electrically conductive layers, and said stress absorption layer being lower in rigidity than said plural generally column shaped electrically conductive layers, and said stress absorption layer surrounding said plural generally column shaped electrically conductive layers so that said stress absorption layer is in tightly contact with said plural generally column shaped electrically conductive layers.

30. The semiconductor device as in 29, wherein said plural generally column shaped electrically conductive layers are made of a metal.

31. The semiconductor device as in 29, wherein said stress absorption layer is made of an organic insulative material.

32. The semiconductor device as in 18, wherein said buffer layer comprises

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode;

a supporting plate 22 having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board ; and

a supporting sealing resin material 22 filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

33. The semiconductor device as in 32, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

34. The semiconductor device as in 32, wherein said plural generally column shaped electrically conductive layers are made of a metal.

35. The semiconductor device as in 32, wherein said supporting sealing resin material is made of an organic insulative material.

36. The semiconductor device as in 18, further comprising a supporting layer 34 on said second surface of said buffer layer for supporting said external electrode.

43. A semiconductor device comprising an interconnection board having first and second surfaces;

at least a semiconductor chip mounted on said interconnection board; external electrodes fixed to external electrode pads on said second surface of said interconnection board; and a supporting layer 22 on said second surface of said interconnection board for supporting said external electrodes.

50. The semiconductor device as in 43, wherein said external electrodes connected through plural generally column shaped

electrically conductive layers to external electrode pads on said second surface of said interconnection board, and said supporting layer further comprises

a supporting plate 22 having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board; and

a supporting sealing resin material 22 filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

51. The semiconductor device as in 50, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

52. The semiconductor device as in 50, wherein said plural generally column shaped electrically conductive layers are made of a metal.

53. The semiconductor device as in 50, wherein said supporting sealing resin material is made of an organic insulative material.

55. The semiconductor device as in 43, wherein said external electrode comprises a pin electrode.

56. The semiconductor device as in 43, wherein said external electrode comprises a coil-spring electrode.

57. The semiconductor device as in 18, wherein said external electrode comprises a generally column shaped electrode.

58. The semiconductor device as in 24, wherein said generally column shaped electrode comprises a straight column shaped electrode which is uniform in horizontal cross sectional area from a bottom to a top thereof.

59. The semiconductor device as in 24, wherein said generally column shaped electrode comprises a center-pinched column shaped electrode which decreases in horizontal cross sectional area toward an intermediate level thereof.

Although Allen teaches a chip mounted on the interconnection board, Allen does not appear to explicitly teach

a chip mounted on the first surface of the board, or the following:

19. The semiconductor device as in 18, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

21. The semiconductor device as in 18, wherein said external electrode comprises a solder ball.

38. The semiconductor device as in 18, wherein said at least semiconductor chip is bonded via bumps to said second surface of said interconnection board.

39. The semiconductor device as in 38, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

40. The semiconductor device as in 39, further comprising at least a heat spreader provided on said at least semiconductor chip.

41. The semiconductor device as in 38, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

42. The semiconductor device as in 41, further comprising a stiffener extending on a peripheral region of said buffer layer;

and at least a heat spreader provided on said at least semiconductor chip and on said stiffener.

45. The semiconductor device as in 43, wherein said at least semiconductor chip is bonded via bumps to said second surface of said interconnection board.

46. The semiconductor device as in 45, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

47. The semiconductor device as in 46, further comprising at least a heat spreader provided on said at least semiconductor chip.

48. The semiconductor device as in 45, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

54. The semiconductor device as in 43, wherein said external electrode comprises a solder ball.

Nonetheless, at column 4, line 59 to column 8, line 61, Tsukamoto teaches a semiconductor device wherein an interconnection board 101 comprises a multilayer interconnection board having a multilevel interconnection structure, an external electrode comprises a solder ball, a semiconductor chip 201 is

bonded via bumps 204 to a first surface of the interconnection board, a sealing resin 205 material provided on the first surface of the interconnection board for sealing the semiconductor chip and the bumps, an under-fill resin material 205 provided on the first surface of the interconnection board for sealing the at least semiconductor chip and the bumps, a stiffener 106 extending on a peripheral region of the interconnection board; and at least a heat spreader 701 provided on the semiconductor chip and on the stiffener. Moreover, it would have been obvious to combine the invention of Tsukamoto with the invention of Allen because it would provide a chip carrier.

The prior art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist whose telephone number is 703-308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/305-3431.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
28-Feb-02